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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	NVID-P003124	5788

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EXAMINER	
MYERS, PAUL R	
ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/847,991	KIM ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/17/09 have been fully considered but they are not persuasive.

In regards to applicants argument that Zucker fails to teach or suggest the limitation of "wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources,": This is clearly incorrect. Zucker teaches the first resource controller (80) is operable to implement a first bus (connection from first processors middle item 70 to the resource controllers crossbar 84) for enabling first communication between a first processor (one of the processors 10) of said plurality of processors (10) and first memory resource (one of the memories coupled to 84 via 76) of said plurality of memory resources (all the memories coupled to 84 via 76)

In regards to applicants argument that Zucker fails to teach or suggest the limitation of "wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources": This is clearly incorrect. Zucker teaches the first resource controller (80) is operable to implement a second bus (connection from second processors middle item 70 to the resource controllers crossbar 84) for enabling second communication between a second processor (another one of the processors 10) of said plurality of processors (10) and second memory resource (another one of the memories coupled to 84 via 76) of said plurality of memory resources (all the memories coupled to 84 via 76).

In regards to applicants argument that Zucker fails to teach or suggest the limitation of "wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication": The examiner notes the claim language does not require simultaneous communication only independent communication. The fact that Zucker uses different buses makes the communication independent.

In regards to applicants argument that Zucker implements a shared bus since Zucker teaches a demultiplexer. The examiner notes Zuckers' "demultiplexers" has two inputs and a plurality of outputs. A demultiplexer with multiple inputs and multiple outputs is called a crosspoint switch. This however does not alleviate the fact that Zucker expressly shows separate buses in figure 8.

In regards to applicants argument that applicants fails to find any teaching or suggestion of independent communication over the first and second bus as claimed: The first bus is only attached to the first processor and the two OSN's 84 (at a first connection point) and the second bus is only attached to the second processor and the two OSN's 84 (at a second connection point). The two processors operate independently only sharing the lock mechanism that prevents them from accessing the same memory at the same time. Thus the communications over the busses connecting them to the OSN's has no choice but to be independent.

In regards to applicants argument that Zucker fails to teach simultaneous accessing different memories While the teaching of not accessing the same memory at the same time implies they can access different memories at the same time this is moot since the claim language only requires independent communication not simultaneous communication.

In regards to applicants argument that Frankeny either alone or in combination with Zucker fails to cure the deficiencies of Zucker discussed herein: While Zucker expressly shows the two separate buses thus is not deficient. The examiner notes that Frankeny et al expressly shows a cross-bar switch allowing simultaneous communication as well as direct communication between the processors, thus if Zucker were deficient, Frankeny would clearly make it obvious to provide separate paths to allow independent communications and in fact allow simultaneous communication. For those claims that require simultaneous communication Frankeny et al will now be applied.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 28-29, 32-33, 35, 37-38, 41-42, 44, 46-47, 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Zucker et al PN 3,805,247.

In regards to claims 28, 37, 46, 48: Zucker et al teaches a system (Figure 8) comprising: a plurality of memory resources (memories attached to 76); a plurality of peripheral resources (Devices attached to 76); a plurality of processors (10); a memory controller (80, 84 and 86) coupled to said plurality of processors (10) and said plurality of memory resources (memories attached to 76), wherein said memory controller comprises a first resource controller (80) for controlling access of said plurality of processors (10) to said plurality of memory resources

(memories attached to 76), wherein said first resource controller (80) is further operable to implement a first bus (connection from second processors middle item 70 to the resource controllers OSN 84) for enabling first communication between a first processor (10) of said plurality of processors and a first memory resource of said plurality of memory resources, wherein said first resource controller (80) is further operable to implement a second bus (connection from second processors middle item 70 to the resource controllers OSN 84) for enabling second communication between a second processor (10) of said plurality of processors and a second memory resource of said plurality of memory resources, and wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication (the communications are independent they are using different buses); and a peripheral controller (82, 84 and 86) coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller (82) for controlling access of said plurality of processors to said plurality of peripheral resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources (84 and 86 are crossbar switches).

In regards to claims 29, 38: Zucker et al teaches a timer component (Clock 20 and 53) coupled to the controllers to control timing of the controllers.

In regards to claims 32, 41: Zucker teaches the processors performing operations in parallel.

In regards to claims 33, 42, 47: Zucker teaches a semaphore (Lock Column 12 lines 18-32).

In regards to claims 35, 44: Zucker teaches the priority scheme being round robin (revolving priority Column 8 lines 11-21)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 30-31, 34, 39-40, 43, 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zucker et al PN 3,805,247 in view of Frankeny et al PN 5,949,982.

In regards to claims 30-31, 39-40, 49-50: Zucker teaches preventing accessing to the same resource at the same time implying accessing of different memories and different peripherals at the same time. (Column 11 line 28-43 and Column 10 line 41 to column 11 line 59). Zucker however does not expressly state that simultaneous access to different memories is performed. Frankeny expressly teaches simultaneous communications to different resources (Abstract). It would have been obvious to allow simultaneous communications to different resources in the system of Zucker because this would have prevented stalling a processor to access a resource that is not in use.

In regards to claims 34, 43: Zucker teaches the processors communicating through crossbar switches to memories and devices via cross bar switches. Zucker however does not expressly teach the processors being able to communicate with each other. Zucker does teach them both being able to access the lock to determine if the other processor is accessing the

desired shared resource. Frankeny et al teaches a plurality of processors communicating to each other and a plurality of memories and a plurality of I/O devices via a crossbar switch. It would have been obvious to allow the processors to also communicate with each other because this would have allowed for functions such as symmetrical multiprocessing.

6. Claims 36, 45, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zucker et al PN 3,805,247.

In regards to claims 36, 45 and 51: Zucker teaches the claimed computer system. Zucker however does not teach the system is portable. Official notice is taken that portable computers are well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include Zucker et al's design in a portable computer because this would have made it portable.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul R. Myers
Primary Examiner
Art Unit 2111

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